Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (*Previously Presented*) A configurable circuit arrangement comprising at least one circuit component at which a load is applied that can vary during operation of said circuit arrangement, wherein said configurable circuit arrangement comprises:

load determination means for determining a load applied at said at least one circuit component having different fan-in or fan-out depending on a configuration of said configurable circuit arrangement; and

adjusting means for switching off a buffer connected to the at least one circuit component according to the determination of the applied load, wherein switching off the buffer adjusts a drive capacity of said at least one circuit component to a value less than a maximum drive capacity while still meeting a delay specification.

2. (*Previously Presented*) A configurable circuit arrangement according to claim 1, wherein said determination means is configured to determine said load based on a configuration information loaded to said configurable circuit arrangement.

3. (*Cancelled*)

4. (*Previously Presented*) A configurable circuit arrangement according to claim 2, wherein said configuration information comprises a configuration bit stream defining at least one of an input load and an output load of said at least one circuit component.

5. (*Cancelled*)

6. (*Cancelled*)

7. (*Previously Presented*) A configurable circuit arrangement according to claim 1, wherein said adjusting means is adapted to generate at least one control signal for simultaneously switching off a section of buffers.

8. (*Previously Presented*) A configurable circuit arrangement according to claim 7, wherein said adjusting means is adapted to derive said control signal from a most significant bit signal of a selection signal obtained from said determination means.

9. (*Previously Presented*) A configurable circuit arrangement according to claim 1, wherein said adjusting means is configured to vary a threshold voltage of circuit elements of said configurable circuit arrangement.

10. (*Previously Presented*) A configurable circuit arrangement according to claim 9, wherein said adjusting means is adapted to change at least one bias voltage responsive to said determination means.

11. (*Previously Presented*) A configurable circuit arrangement according to claim 1, wherein said configurable circuit arrangement is a field programmable gate array device.

12. (*Cancelled*)

13. (*Cancelled*)

14. (*Cancelled*)

15. (*Previously Presented*) A configurable circuit arrangement comprising:

at least one circuit component at which a load is applied that can vary during operation of said configurable circuit arrangement;

load determination means for determining a load applied at said at least one circuit component, wherein the at least one circuit component has different fan-in or fan-

out depending on a configuration of said configurable circuit arrangement, wherein said determination means is configured to determine said load based on a configuration information loaded to said configurable circuit arrangement, wherein said configuration information is stored in a configuration memory; and

adjusting means for switching off a buffer connected to the at least one circuit component according to the determination of the applied load, wherein switching off the buffer adjusts a drive capacity of said at least one circuit component to a value less than a maximum drive capacity while still meeting a delay specification.

16. (*Previously Presented*) A configurable circuit arrangement according to claim 15, wherein said configuration information comprises a configuration bit stream defining at least one of an input load and an output load of said at least one circuit component.

17. (*Previously Presented*) A configurable circuit arrangement according to claim 15, wherein said adjusting means is adapted to generate at least one control signal for simultaneously switching off a section of buffers.

18. (*Previously Presented*) A configurable circuit arrangement according to claim 17, wherein said adjusting means is adapted to derive said control signal from a most significant bit signal of a selection signal obtained from said determination means.

19. (*Previously Presented*) A configurable circuit arrangement according to claim 15, wherein said adjusting means is configured to vary a threshold voltage of circuit elements of said configurable circuit arrangement.

20. (*Previously Presented*) A configurable circuit arrangement according to claim 19, wherein said adjusting means is adapted to change at least one bias voltage responsive to said determination means.

21. (*Previously Presented*) A configurable circuit arrangement according to claim 15, wherein said configurable circuit arrangement comprises a field programmable gate array device.